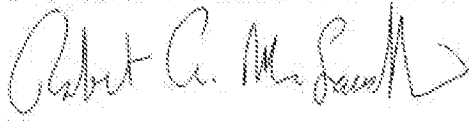


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: John Gregory Ferrara
Serial No. 10/720,785
Filing Date: November 24, 2003
Group Art Unit: 2115
Examiner: Patel, Hari
Title: AN ON-CHIP REALTIME CLOCK MODULE

Mail Stop: Non-Fee Amendments
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

<p align="center"><u>Certification Under 37 C.F.R. 1.8</u></p> <p><u>Date of Mailing or Facsimile Transmission: December 11, 2006</u></p> <p>I hereby certify that this correspondence is being deposited with the United States Postal Service via First Class Mail with sufficient postage for mailing under 37 CFR § 1.8 on the date indicated above and addressed to the Mail Stop: Amendments, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office at 571-273-8300 under 37 CFR § 1.8 on the date indicated.</p> <p align="center"></p> <p align="center">_____ Robert A. McLachlan</p>

AMENDMENT

Dear Sir:

In response to the Official Action mailed June 15, 2006, Applicant respectfully requests the Examiner reconsider the rejections of the Claims in view of the following amendments to the Specification and Claims and comments as set forth below.

Please replace paragraph [0026] with paragraph [0026] on page 2 of this amendment.

[0026] With the multi-function handheld device 10 in the first functional mode, the integrated circuit 12 facilitates the transfer of data between the host device A, B, or C and memory 16, which may be non-volatile memory (e.g., flash memory, disk memory, SDRAM) and/or volatile memory (e.g., DRAM). In one embodiment, the memory IC 16 is a NAND flash memory that stores both data and the operational instructions of at least some of the algorithms 30. The interoperability of the memory IC 16 and the integrated circuit 12 will be described in greater detail with reference to FIGUREs 7-10.